TMS320F240 DSP
EVALUATION BOARD
User's Manual

DSK-DSP-240Q

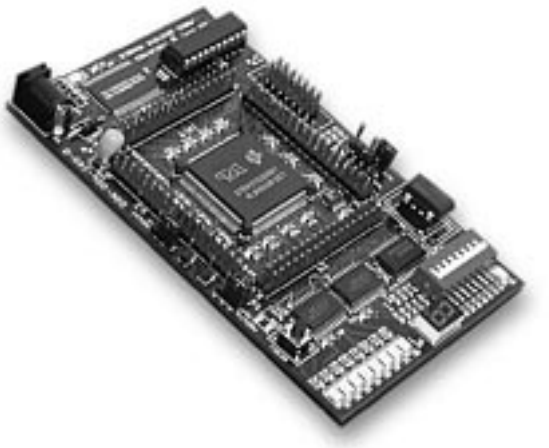

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Table of Contents

1 Introduction

DSK-DSP-240Q is a general purpose Evaluation Module (EVM) built around the Texas Instruments TMS320F240 Digital Signal Processor (DSP).

The EVM offers an affordable way of evaluating and exploring the architecture of the C24x family of DSP controllers, which are optimized for motor-control and power conversion applications. The board is controlled via the JTAG connector of Signum Systems' JDSnet-2xx emulator, which in turn is connected to your PC's parallel port (LPT1 or LPT2). The emulator and evaluation board, together with Signum Systems' Chameleon Debugger, allow for real-time execution, verification and debugging of your C24x code. The four 36-pin connector headers placed around the DSP may be used to plug in real-time trace modules, external peripheral expansion boards, prototyping boards, etc.

The DSK-DSP-240Q comes with the following features:

- TMS320F240 fixed-point DSP controller with 544 words of RAM, dual 10-bit A/D converter, serial port, 3 timers, 12 PWM channels, 4 capture units, watchdog and 28 I/O pins
- 64K words of external static RAM
- Bank of eight LEDs
- 7-segment display
- Bank of eight DIP switches
- XF flag LED
- RESET pushbutton switch
- Four 34-pin expansion / real-time trace connectors
- 14-pin JTAG emulation port

2 Installation

2.1 System Requirements

HARDWARE REQUIREMENTS:

- Host PC capable of running the Chameleon Debugger (Pentium PC with CD-ROM, 64MB RAM, 20MB free hard disk space)
- Parallel port to connect the JDSnet emulator. The EPP mode is supported and recommended for faster downloads, so please make sure your parallel port is configured for the EPP mode of operation.

SOFTWARE REQUIREMENTS

- Windows 95, 98, 2000 or NT
- Chameleon Debugger for the TMS320C2xx family (CHDEB-2xx-JDS)
- C or ASM language cross compiler for the TMS320C2xx family is required for software development or modification of included sample code.

2.2 Hardware Installation

Your package should contain the following:

- DSK-DSP-240Q evaluation board
- AC adapter
- Floppy diskette with sample software and documentation
- *TMS320F240 DSP Evaluation Board User's Manual: DSK-DSP-240Q* document
- Any optional items ordered

2.3 Connecting the Evaluation Board

In order to use the EVM board with emulator, the emulator and Chameleon Debugger software must be installed first. Please follow the debugger installation instructions first. Once the emulator and debugger are installed, please follow the steps below to connect the EVM board to the emulator:

1. Exit the debugger software (if running).
2. Turn the emulator power switch OFF.
3. Connect the parallel cable between the emulator and your PC.
4. Connect the 14-pin JTAG header on the emulator to the 14-pin JTAG emulation port on the DSK-DSP-240Q board (the connector is keyed for proper connection).
5. Connect the AC adapter to the AC outlet and to the EVM board power connector.
6. Turn on the power to the JDSnet emulator.
7. Start the Chameleon Debugger.

If the Chameleon Debugger was installed properly for the TMS320C2xx target and parallel port, the debugger screen should display the following messages in the SYSLOG window:

3 DSK-DSP-240Q Features

3.1 Memory

The DSK-DSP-240Q evaluation board contains a total of 64K words of external SRAM memory. The 64K*16 memory spans the entire external program memory space of the DSP from 0 to 0xFFFF. The upper 32K words of external program memory (0x8000 to 0xFFFF) is shared with external data memory space.

EXTERNAL PROGRAM MEMORY

To use the external program or data memory the MP/MC- shunt must be in the 1-2 for the ’F240 device to operate in microprocessor mode.

When the ‘F240 device is operating in the microcomputer mode, only program memory accesses above 0x4000 reside in external program memory. All program memory accesses at or below 0x4000 reside in the 16K words of on-chip Flash memory. The MP/MC jumper (JP1) must be in position 2-3 for the ‘F240 device to operate in the microcomputer mode.

	MP mode	MC mode
External Program Memory	0x0000 – 0xFFFF	0x4000 – 0xFFFF

If your program uses the entire 64K words of program space, the data memory must be fitted entirely in the 544 words of on-chip memory. If the program space is less than 64K, the remaining external memory may be used as external data memory in addition to the 544 words in on-chip data memory.

EXTERNAL DATA MEMORY

External data memory accesses for the ‘F240 device are only valid for the upper 32K words (0x8000 – 0xFFFF) of local data memory space.

Caution: The lower 32K words (0 to 0x7FFF) of external data memory space are reserved for on-chip peripheral registers and memory-mapped registers of the DSP.

Even thought the ‘F240 devices are capable of addressing separate external program and data memory spaces, for simplicity, the DSK-DSP240Q combined the upper 32K memory spaces into one 32K space. As a result, the upper 32K of external data memory is shared with the upper 32K of external program memory.

	MP or MC mode
External Data Memory	0x8000 – 0xFFFF (shared with program memory)

For simplicity reasons, the global memory allocation register (GREG) does not have an effect on the data memory configuration and will be ignored.

3.2 Analog-to-Digital Converter

The ‘F240 device has an on-chip, dual, 10-bit analog-to-digital converter (ADC) module. The ADC module consists of two 10-bit ADCs with two internal sample-and-hold circuits. Eight analog inputs are provided for each ADC unit via an 8-to-1 analog multiplexer. The maximum conversion time for each ADC unit is 6.6 ms. See the *Dual 10-Bit Analog to Digital Converter (ADC) Module* section in Volume 2 of *TMS320C240 DSP Controllers Reference Set* for more details on the on-chip ADC module.

The reference voltages for the ADC module must be supplied from an external source. The VREFHI (JP32) and VREFLO (JP4) jumpers allow you to set the upper and lower references anywhere between 0 and 5 V dc. When the JP3 and JP4 jumpers are in position 1–2, VREFHI is connected directly to the 5V power plane and VREFLO is connected directly to the ground plane. When jumpers JP3 and JP4 are in position 2–3, the upper and lower references can be supplied by external voltage references connected to test points J3 and J4 respectively.

All analog signals must be input to the ‘F240 device through the P2 and P3 headers located right next to the DSP.

3.3 Watchdog Timer (WD)

The ‘F240 DSP contains on-chip watchdog timer (WD) that starts running automatically after power-up or RESET. The timer protects against system software failures and CPU

disruption by providing a system reset when WDKEY register is not serviced before a watchdog overflow.

The typical WDCLK overflow frequency is 16 384 Hz.

SERVICING THE WD TIMER

The WDCNTR is reset when the proper sequence is written to the WDKEY before the WDCNTR overflows.

The WDCNTR is enabled for reset when a value of **55h** is written to the WDKEY. When the next **AAh** value is written to the WDKEY, then the WDCNTR actually is reset. Any value written to the WDKEY other than 55h or AAh causes a system reset.

All example programs supplied with the evaluation board contain WD service routines. Please use them as a guide when writing your own software for the ‘F240 device.

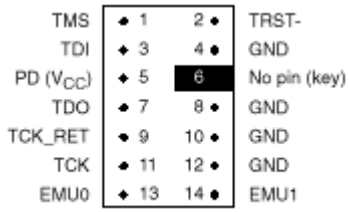
WD DISABLE

For development purposes, the WD timer can be disabled by applying 5V to the VCCP pin (move jumper J2 to position 1-2) during the device reset sequence and setting the **WDDIS bit** in the WD control register (WDCR.6). However, if the hardware and software conditions are not met, the WD timer will not be disabled.

3.4 Connectors

EMULATION PORT

The 14-pin JTAG emulation port (P5) allows the evaluation board to be controlled by the JDSnet emulator. This port is based on the IEEE 1149.1 standard and is accessed by the emulator. The evaluation board, which serves as the target system, has a 14-pin header (two rows of seven pins) with the connections shown below to communicate with either the JDSnet or XDS510 emulator.



TRACE / EXPANSION CONNECTORS

The four 34-pin connectors (P1, P2, P3, P4) around the DSP give you full access to every signal on the ’F24x device. These connectors are mainly used for attaching the real-time trace buffer to the JDSnet emulator, but may also be used for adding additional custom boards with other peripherals to the DSK-DSP-240Q evaluation board.

The connectors are laid out according to the ‘F240 pin out so that each 34-pin connector picks–up signals from one side of the DSP. Please refer to the schematic in the Appendix for the pinout of P1, P2, P3 and P4 trace/expansion connectors.

POWER SUPPLY

The power supply included with the EVM delivers 5V DC at 300 mA and mates with the J5 power plug. If any custom modules are attached to the EVM, replace the power supply with one that will supply enough power for the entire project.

3.5 Jumpers

There are four jumpers on the DSK-DSP-240Q evaluation board for you to configure. These jumpers set the analog reference voltages, Flash programming/watchdog disabling and MP or MC mode of operation.

Table below summarizes the function of each jumper on the evaluation board. Each entry in the table gives the jumper name, jumper number, and the resulting function when it is in a given position. Refer to this table when configuring the jumpers on the EVN-240Q evaluation board.

Jumper Name	Reference	Position	Description
MP / MC	JP1	1-2	The 'F240 device runs in the microprocessor mode and makes all program memory accesses off-chip.
		2-3	The 'F240 device runs in the microcontroller mode and makes program memory accesses below 0x4000 from on-chip Flash memory.
VPP WDE	JP2	1-2	The Flash array can be programmed and the watchdog is disabled when WDCR.6 is set.
		2-3	The Flash array cannot be programmed and the watchdog is enabled.
VREFLO	JP3	1-2	The on-chip ADC VREFLO signal is tied directly to the ground.
		2-3	The on-chip ADC VREFLO signal is tied to test point J3 for use with external reference.
VREFHI	JP4	1-2	The on-chip ADC VREFHI signal is tied directly to the 5V power
		2-3	The on-chip ADC VREFHI signal is tied to test point J4 for use with external reference.

3.6 LEDs

There are ten LEDs on the 'C24x evaluation board. These LEDs display such information as board power, the status of the XF pin, and the status of certain bits mapped into the I/O memory space. The bank of eight LEDs on the evaluation board is mapped to location 0x000C and the 7-segment digit display to the location 0x000D in the I/O memory space of the 'F240 device.

Each of the eight LEDs can be turned on and off independently by setting or clearing the specific bit assigned to that individual LED. The following instructions may be used to turn OFF all eight LEDs by setting the eight LSBs in the LEDS register and writing it to location 0x00C in I/O space:

```
SPLK    #00FFh, LEDS
OUT     LEDS, 000Ch
```

The following instructions can be used to turn ON all eight LEDs by clearing the eight LSBs in the LEDS register and writing it to location 0x000C in I/O space:

```
SPLK    #0000h,LEDS
OUT     LEDS, 000Ch
```

Because of the pin limitation of the address decoder (GAL16V8 at U8), the LEDs can also be changed by writing to any I/O location that ends with C or D in the lower 32K of the I/O space. Thus, I/O addresses 0x001C, 0x002C through 0x7FFC are also able to change the state of the 8 LEDs, while locations 0x001D through 0x7FFD are able to change the 7-Sgement display.

The I/O-mapped LEDs are considered write-only devices by the ’F240. Therefore, the correct status of the LED register or 7-Segement display is not reflected when reading address 0x000C or 0x000D in I/O space.

The following table summarizes the function of each LED on the evaluation board.

LED Name	Status	Description
Power	On	+5V power is supplied to the board
	Off	No power is supplied to the board
XF	On	The XF flag is set to 1
	Off	The XF flag is set to 0
D1-D8	On	When the data written to I/O loc. 0xC is 0
	Off	When the data written to 0xC is 1
7-Segment Display		When the data written to I/O loc. 0xD is:
	1	1FH
	2	42H
	3	0AH
	4	19H
	5	88H
	6	80H
	7	1EH
	8	00H
	9	08H
	0	04H

3.7 Switches

DIP SWITCH (SW1)

The bank of eight DIP-switches (SW1) on the evaluation board maps to location 0x0008 in the I/O memory space of the ’F240 device.

The following assembly instruction may be used to read the bank of DIP switches into the SWITCH variable:

```
IN      SWITCH, 0008h
```

Because of the pin limitation of the address decoder (GAL16V8 at U8), the DIP switch can also be read by reading any I/O location that ends with 8 in the lower 32K of the I/O space. Thus, I/O addresses 0x0018, 0x0028, etc. through 0x7FF8 are also able to read the state of the DIP switch.

RESET SWITCH (U12)

The RESET switch is connected to the RS’ input of the ‘F240 device and will generate a reset when pressed.

3.8 DSP Clock

The evaluation board contains a 10 MHz socketed clock generator to drive the ‘F240 DSP device. To allow the use of clock generator, the OSCBYP’ pin of the DSP is tied to ground.

When the board first powers up, the device is running off the CLKIN clock divided-by-2 (CLKMD = 00). To run the DSP at the full 20 MHz frequency, the CLKMD register bit 0 must be set to 1 (CLKMD = 01). The easiest way to change the DSP clock would be to replace the 10 MHz clock generator. If this is inconvenient, different CPUCLK rates may be obtained by programming the on-chip PLL Clock Module.

Caution: ‘F240 devices are designed to run at up to 20 MHz CPUCLK. While selecting PLL register values, care should be taken to limit the CPUCLK rate to 20 MHz maximum.

4 Appendices

4.1 Appendix A: Specifications

Size	4.8 in x 3.0 in
Power	5V DC @ 500 mA
Processor Type	TMS320F240 (132 PQFP)
Clock IN/SYSCLK	10 MHz (removable)
External Program Memory	64K words (0 to 0xFFFF)
External Data Memory	32K (0x8000 to 0xFFFF) shared with External Program Memory
LEDs	Power On Bank of 8 (I/O loc. 0x000C) 7-Segemt (I/O loc. 0x000D XF
Switches	DIP switch (I/O loc. 0x0008) RESET
Jumpers	MP/MC VPP/WDE VREFLO VREFHI
Connectors	JTAG (14-pin) Trace/Expansion (4 x 34-pin)
	32K x 80 bits

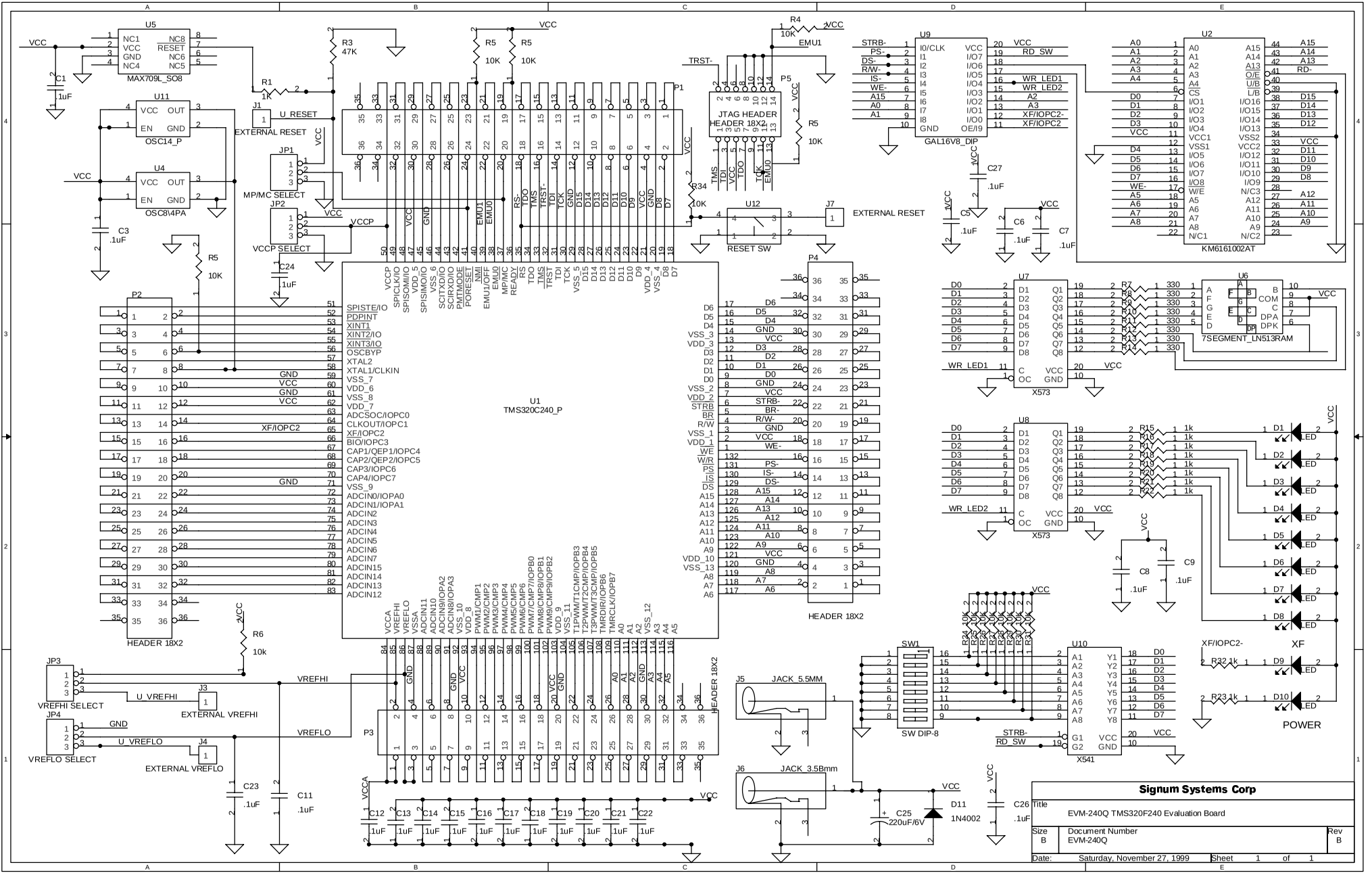
4.2 Appendix B: Schematic

PARTS LIST

Qty.	Description	Part Reference(s)
23	0.1uF	C1, C3, C5-C9, C11-24, C26-27
1	220uF/6V	C25
10	LED	D1-D10
1	1N4002	D11
1	EXTERNAL RESET	J1
1	EXTERNAL VREFHI	J3
1	EXTERNAL VREFLO	J4
1	JACK_5.5MM/3.5	J5/J6
1	EXTERNAL RESET	J7
1	MP/MC SELECT	JP1
1	VCCP SELECT	JP2
1	VREFHI SELECT	JP3
1	VREFLO SELECT	JP4
4	HEADER 18X2	P1-P4
1	JTAG HEADER	P5
1	47K	R3
1	330	R7-R14
11	1K	R1, R15-R23, R32
12	10K	R4-R6, R24-R31, R34
1	SW DIP-8	SW1
1	TMS320F240_P	U1
1	KM6161002AT	U2
1	OSC 20MHz	U4/U11
1	MAX709L_SO8	U5
1	LN513RAM	U6
2	X573	U7, U8
1	GAL16V8_DIP	U9
1	X541	U10
1	RES SWITCH	U12

SCHEMATIC

A schematic of the pod is shown on the insert.


U1
TMS320C240_P
HEADER 18X2
P1
P2
P3
P4
P5
U2
KM6161002AT
U3
U4
OSC14_P
OSC8I4PA
U5
MAX709L_SO8
U6
7SEGMENT_LN513RAM
U7
U8
X573
U9
GAL16V8_DIP
U10
X541
U11
U12
RESET SW
JTAG HEADER
HEADER 18X2
R1
1K
R2
R3
47K
R4
10K
R5
10K
R6
10k
C1
.1uF
C2
C3
.1uF
C4
.1uF
C5
.1uF
C6
.1uF
C7
.1uF
C8
.1uF
C9
.1uF
C10
.1uF
C11
.1uF
C12
1uF
C13
1uF
C14
1uF
C15
1uF
C16
1uF
C17
1uF
C18
1uF
C19
1uF
C20
1uF
C21
1uF
C22
1uF
C23
.1uF
C24
.1uF
C25
220uF/6V
C26
.1uF
C27
.1uF
D11
1N4002
J1
EXTERNAL RESET
J2
VCCP SELECT
J3
EXTERNAL VREFHI
J4
EXTERNAL VREFLO
J5
JACK_5.5MM
J6
JACK_3.5Bmm
J7
EXTERNAL RESET
JP1
MP/MC SELECT
JP2
VCCP SELECT
JP3
VREFHI SELECT
JP4
VREFLO SELECT
SW1
SW DIP-8
R7
330
R8
330
R9
330
R10
330
R11
330
R12
330
R13
330
R14
330
R15
1k
R16
1k
R17
1k
R18
1k
R19
1k
R20
1k
R21
1k
R22
1k
R23
1k
R24
10K
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R26
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R29
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R31
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R34
10K
D1
LED
D2
LED
D3
LED
D4
LED
D5
LED
D6
LED
D7
LED
D8
LED
D9
LED
D10
LED
VCC
VCCP
GND
RESET
EMU1
EMU0
TRST-
TMS
TDI
TDO
TCK
TCK2
EMU0
EMU1
RS-
XF/IOPC2
XF/IOPC2-
XF
POWER
WR_LED1
WR_LED2
RD_SW
STRB-
PS-
DS-
R/W-
IS-
WE-
A15
A0
A1
U_RESET
U_VREFHI
U_VREFLO
VREFHI
VREFLO
SPISTE/IO
PDPINT
XINT1
XINT2/IO
XINT3/IO
OSCBYP
XTAL2
XTAL1/CLKIN
VSS_7
VDD_6
VSS_8
VDD_7
ADCSOC/IOPC0
CLKOUT/IOPC1
XF/IOPC2
BIO/IOPC3
CAP1/QEP1/IOPC4
CAP2/QEP2/IOPC5
CAP3/IOPC6
CAP4/IOPC7
VSS_9
ADCIN0/IOPA0
ADCIN1/IOPA1
ADCIN2
ADCIN3
ADCIN4
ADCIN5
ADCIN6
ADCIN7
ADCIN15
ADCIN14
ADCIN13
ADCIN12
Signum Systems Corp
EVM-240Q TMS320F240 Evaluation Board
Document Number
EVM-240Q
Rev
B
Size
B
Date:
Saturday, November 27, 1999
Sheet
1
of
1

GAL EQUATIONS

```
Title       DSK-DSP-240Q
Pattern     1
Revision    A
Author      S
Company     Signum Systems Co.
Date        10-22-1999
CHIP        u9 palce16v8

;
Pin 1   /Strb    Comb ; Input
Pin 2   /Ps      Comb ; Input
Pin 3   /Ds      Comb ; Input
Pin 4   /R_W     Comb ; Input
Pin 5   /Is      Comb ; Input
Pin 6   /We      Comb ; Input
Pin 7    A15     Comb ; Input
Pin 8    A0      Comb ; Input
Pin 9    A1      Comb ; Input
Pin 10  GND
Pin 11  XFin     Comb ; Input
Pin 12  XFout    Comb ; Output
Pin 13  A3       Comb ; Input
Pin 14  A2       Comb ; Input
Pin 15  WrLed2   Comb ; Output
Pin 16  WrLed1   Comb ; Output
Pin 17 /RamRd    Comb ; Output
Pin 18 /RamCs    Comb ; Output
Pin 19 /RdSw     Comb ; Output
Pin 20  VCC

Equations
minimize_off
XFout = XFin;
WrLed2 = Is * Strb * R_W * /A15 * A3 * A2 * /A1 * /A0;  0xC
WrLed1 = Is * Strb * R_W * /A15 * A3 * A2 * /A1 *  A0;  0xD
RamRd  = Ps * Strb * /R_W
       + Ds * Strb * /R_W;
RamCs  = Ps + Ds;
RdSw   = Is * Strb * /R_W * /A15 * A3 * /A2 * /A1 * /A0;  0x8
```

4.3 Appendix C: Technical Support

You can contact Signum Systems Technical Support by dialing (805) 523-9774, Monday through Friday between 9 A.M. and 5 P.M. Pacific Time. In order to enable our technical support engineers to process your request efficiently, we strongly recommend submitting the Technical Support Request form available at http://www.signum.com/support.htm. Our support team can also be reached by email at support@signum.com.

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